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Set Name side by side	Query	Hit Count	Set Name result set
	DB=PGPB; PLUR=YES; OP=ADJ		
L8	L4 and source and drain and conduct$ and (pillar or column)	62	L8
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	DB=EPAB; PLUR=YES; OP=ADJ		
L6	semiconductor and (insulat$ adj gate) and trench and spacer	0	L6
	DB=JPAB; PLUR=YES; OP=ADJ		
L5	semiconductor and (insulat$ adj gate) and trench and spacer	1	L5
	DB=PGPB; PLUR=YES; OP=ADJ		
L4	semiconductor and (insulat$ adj gate) and trench and spacer	210	L4
	DB=USPT; PLUR=YES; OP=ADJ		
L3	semiconductor and (insulat$ adj gate) and trench and spacer	550	L3
	DB=TDBD; PLUR=YES; OP=ADJ		
L2	semiconductor and (insulat$ adj gate) and trench and spacer	0	L2
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L1	semiconductor and (insulat$ adj gate) and trench and spacer	15	L1

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Search Results - Record(s) 1 through 15 of 15 returned.

☐ 1. Document ID: EP 1191603 A2 JP 2002217426 A US 6396090 B1 CN 1348220 A

L1: Entry 1 of 15 File: DWPI Mar 27, 2002

DERWENT-ACC-NO: 2002-342397
DERWENT-WEEK: 200255

TITLE: Termination structure of trench MOS device, has conductive electrodes formed on either surfaces of substrate, where upper surface of substrate extends from active region to oxide layer through spacer

Basic Abstract Text (1):
NOVELTY - A trench with a MOS gate formed as a spacer on its side wall, is formed from boundary of a substrate active region to end of the substrate. A termination structure oxide layer is formed in the trench to cover the portion of spacer and trench bottom. Conductive electrodes are formed on either surfaces of the substrate, where the upper surface of the substrate extends from active region to the oxide layer through the spacer.

Basic Abstract Text (2):
USE - For trench MOS device e.g. double diffused metal oxide semiconductor field effect transistor (DMOSFET), insulated gate bipolar transistor (IGBT) and schottky diode used as power devices in switching mode power supplies and high speed power switching applications e.g. motor drives, switching of communication device, industry automation and electronic automation.

Patent Assignee Terms (1):
GEN SEMICONDUCTOR INC

Patent Assignee Terms (2):
GEN SEMICONDUCTOR TAIWAN LTD

Patent Assignee Terms (1):
GEN SEMICONDUCTOR INC

Patent Assignee Terms (2):
GEN SEMICONDUCTOR TAIWAN LTD

Equivalent Abstract Text (1):
NOVELTY - A trench with a MOS gate formed as a spacer on its side wall, is formed from boundary of a substrate active region to end of the substrate. A termination structure oxide layer is formed in the trench to cover the portion of spacer and trench bottom. Conductive electrodes are formed on either surfaces of the substrate, where the upper surface of the substrate extends from active region to the oxide layer through the spacer.

Equivalent Abstract Text (2):
USE - For trench MOS device e.g. double diffused metal oxide semiconductor field effect transistor (DMOSFET), insulated gate bipolar transistor (IGBT) and schottky diode used as power devices in switching mode power supplies and high speed power switching applications e.g. motor drives, switching of communication device, industry automation and electronic automation.

Standard Title Terms (1):
TERMINATE STRUCTURE TRENCH MOS DEVICE CONDUCTING ELECTRODE FORMING SURFACE SUBSTRATE UPPER SURFACE SUBSTRATE EXTEND ACTIVE REGION OXIDE LAYER THROUGH SPACE

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

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2. Document ID: TW 456049 A

L1: Entry 2 of 15 File: DWPI Sep 21, 2001

DERWENT-ACC-NO: 2002-469906
DERWENT-WEEK: 200250

TITLE: Trench-type metal oxide semiconductor stop structure provides new stop structure with fewer photomasks and reduced processing complexity

Basic Abstract Text (1):
NOVELTY - The present invention provides a trench stop structure which is used in connection with any kind of trench-type metal oxide semiconductor component to form different power transistor structure with high voltage durability, such as Schottky diode, double diffused MOS, or insulated gate bipolar transistor.

Basic Abstract Text (2):
DETAILED DESCRIPTION - The process includes the following steps: forming trenches in the silicon substrate; growing gate oxide; refilling polysilicon layer; forming the spacer by anisotropic etching; depositing the oxide; defining the contact area with photoresist and etching; and, forming the metal layer and photoresist and etching the defining electrode.

Basic Abstract Text (3):
USE - Metal oxide semiconductor component production.

Basic Abstract Text (4):
ADVANTAGE - Since the metal oxide semiconductor structure and the stop structure are formed at the same time, the process is simpler and the number of required photomasks is three, which is less than the stop structure of conventional local oxide layer with guard ring. The trench-type stop structure can make the depletion area of the device planarized during reverse bias operation. The breakdown voltage will not be reduced by the effect of the stop structure, thus increasing the production yield.

Patent Assignee Terms (1):
GEN SEMICONDUCTOR TAIWAN LTD

Patent Assignee Terms (1):
GEN SEMICONDUCTOR TAIWAN LTD

Standard Title Terms (1):
TRENCH TYPE METAL OXIDE SEMICONDUCTOR STOP STRUCTURE NEW STOP STRUCTURE PHOTOMASK REDUCE PROCESS COMPLEX

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

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3. Document ID: US 20010022379 A1 WO 200182380 A2 AU 200147327 A US 6455379 B2

L1: Entry 3 of 15 File: DWPI Sep 20, 2001

DERWENT-ACC-NO: 2001-601882
DERWENT-WEEK: 200267

TITLE: Trench gated power device e.g. trench metal oxide semiconductor field effect transistor, has P-type body regions which are formed by depositing P-type epitaxial layer adjacent to source regions

Basic Abstract Text (1):
NOVELTY - N-type epitaxial layer (101) of thickness and resistivity selected for desired breakdown voltage is covered by P-type epitaxial layer, which has gate trenches filled with P-type material dividing epitaxial layer. N-type epitaxial layer is laid on P-type layer to form source regions (110). P-type body regions (111) are formed by depositing another P-type epitaxial layer adjacent to source region.

Basic Abstract Text (2):
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for process for forming an improved trench gated power device.

Basic Abstract Text (3):
USE - Trench gated power device e.g., trench metal oxide semiconductor field effect transistor (MOSFET) device, insulated gate bipolar transistor (IGBT) and MCT.

Basic Abstract Text (4):
ADVANTAGE - More economical device fabrication is allowed, by the usage of silicon spacer for forming gate and body regions.

Patent Assignee Terms (2):
FAIRCHILD SEMICONDUCTOR CORP

Patent Assignee Terms (2):
FAIRCHILD SEMICONDUCTOR CORP

Equivalent Abstract Text (1):
NOVELTY - N-type epitaxial layer (101) of thickness and resistivity selected for desired breakdown voltage is covered by P-type epitaxial layer, which has gate trenches filled with P-type material dividing epitaxial layer. N-type epitaxial layer is laid on P-type layer to form source regions (110). P-type body regions (111) are formed by depositing another P-type epitaxial layer adjacent to source region.

Equivalent Abstract Text (2):
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for process for forming an improved trench gated power device.

Equivalent Abstract Text (3):
USE - Trench gated power device e.g., trench metal oxide semiconductor field effect transistor (MOSFET) device, insulated gate bipolar transistor (IGBT) and MCT.

Equivalent Abstract Text (4):
ADVANTAGE - More economical device fabrication is allowed, by the usage of silicon spacer for forming gate and body regions.

Standard Title Terms (1):
TRENCH GATE POWER DEVICE TRENCH METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR P TYPE BODY REGION FORMING DEPOSIT P TYPE EPITAXIAL LAYER ADJACENT SOURCE REGION

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments   KWIC | Draw Desc | Image

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☐ 4. Document ID: US 6251749 B1

L1: Entry 4 of 15   File: DWPI   Jun 26, 2001

DERWENT-ACC-NO: 2002-194435
DERWENT-WEEK: 200225

TITLE: Shallow trench isolation formation in IC manufacture, involves arranging inclined side wall spacer to isolation trench region above semiconductor surface and forming conductor overlay on side walls, trench and surface

Basic Abstract Text (1):
NOVELTY - Side wall spacers (130) are arranged on sides of isolation trench region (110) protruding above semiconductor surface. The side wall spacers are inclined towards isolation region from the surface. An overlay is formed on isolation region and the side walls, from semiconductor surface.

Basic Abstract Text (3):
ADVANTAGE - Provides proper control of individual insulated gate field effect transistors in integrated circuit. Reduces current leakage between the source and drain of the transistors used in the IC. Provides smoother topography to which the metal gate is deposited and reduces the vertical thickness of the tungsten during shallow trench isolation process.

Basic Abstract Text (4):
DESCRIPTION OF DRAWING(S) - The figures show the formation of shallow trench isolation with side walls.

Basic Abstract Text (5):
Isolation trench region 110

Basic Abstract Text (6):
Side wall spacer 130 1B, 1C/6

Standard Title Terms (1):
SHALLOW TRENCH ISOLATE FORMATION IC MANUFACTURE ARRANGE INCLINE SIDE WALL SPACE ISOLATE TRENCH REGION ABOVE SEMICONDUCTOR SURFACE FORMING CONDUCTOR OVERLAY SIDE WALL TRENCH SURFACE

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Drawi Desc | Image

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☐ 5. Document ID: JP 2003515954 W WO 200141206 A2 US 20010009800 A1 EP 1171910 A2 US 6498071 B2

L1: Entry 5 of 15 File: DWPI May 7, 2003

DERWENT-ACC-NO: 2001-625263
DERWENT-WEEK: 200331

TITLE: Trench-gate semiconductor device manufacture involves forming source and drain regions separated by channel-accommodating body region adjacent to trench-gate

Basic Abstract Text (2):
(a) forming a mask having an opening on a semiconductor body (10),

Basic Abstract Text (3):
(b) etching a trench (20) into the semiconductor body at the opening to extend through the body region and into an underlying portion of the drain region,

Basic Abstract Text (4):
(c) providing gate material (11') in the trench and in the window such that the gate

material forms a protruding step from the adjacent surface of the semiconductor body with the mask still present,

Basic Abstract Text (5):
(d) forming a side wall spacer (32) in the step to replace the mask,

Basic Abstract Text (6):
(e) forming the source region (13) with a lateral extent from the trench being determined by the spacer,

Basic Abstract Text (9):
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for the semiconductor device.

Basic Abstract Text (10):
USE - For the manufacture of metal oxide semiconductor field effect transistor or insulated gate bipolar transistor.

Basic Abstract Text (11):
ADVANTAGE - Permits the use of a side wall spacer at the trench-gate structure for self-aligned formation of the source region while providing a simple process with better definition of the source region.

Basic Abstract Text (12):
DESCRIPTION OF DRAWING(S) - The drawing shows a cross-sectional view of transistor cell areas of a semiconductor body at a stage of manufacture.

Basic Abstract Text (13):
Semiconductor body 10

Basic Abstract Text (16):
Trench 20

Basic Abstract Text (18):
Side wall spacer 32

Equivalent Abstract Text (2):
(a) forming a mask having an opening on a semiconductor body (10),

Equivalent Abstract Text (3):
(b) etching a trench (20) into the semiconductor body at the opening to extend through the body region and into an underlying portion of the drain region,

Equivalent Abstract Text (4):
(c) providing gate material (11') in the trench and in the window such that the gate material forms a protruding step from the adjacent surface of the semiconductor body with the mask still present,

Equivalent Abstract Text (5):
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Equivalent Abstract Text (6):
(e) forming the source region (13) with a lateral extent from the trench being determined by the spacer,

Equivalent Abstract Text (9):
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for the semiconductor device.

Equivalent Abstract Text (10):
USE - For the manufacture of metal oxide semiconductor field effect transistor or insulated gate bipolar transistor.

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ADVANTAGE - Permits the use of a side wall spacer at the trench-gate structure for self-aligned formation of the source region while providing a simple process with better definition of the source region.

Equivalent Abstract Text (12):
DESCRIPTION OF DRAWING(S) - The drawing shows a cross-sectional view of transistor cell areas of a semiconductor body at a stage of manufacture.

Equivalent Abstract Text (13):
Semiconductor body 10

Equivalent Abstract Text (16):
Trench 20

Equivalent Abstract Text (18):
Side wall spacer 32

Standard Title Terms (1):
TRENCH GATE SEMICONDUCTOR DEVICE MANUFACTURE FORMING SOURCE DRAIN REGION SEPARATE CHANNEL ACCOMMODATE BODY REGION ADJACENT TRENCH GATE

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw. Desc | Image

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6. Document ID: US 6201278 B1

L1: Entry 6 of 15 File: DWPI Mar 13, 2001

DERWENT-ACC-NO: 2001-396281
DERWENT-WEEK: 200142
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TITLE: Insulated gate field effect transistor, has oxide spacers that are set between the non-floating gate electrode and the opposing sidewalls of the trench

Basic Abstract Text (1):
NOVELTY - Oxide spacers (122A,122B) are set between the gate electrode and the sidewalls of the trench, the spacers having upper surfaces that are coplanar with the surface of the gate electrode. Oxide segments (126A,126B) are set adjacent to the oxide spacers, the segments having upper surfaces that are coplanar with that of the spacers and the gate electrode, respectively.

Basic Abstract Text (2):
DETAILED DESCRIPTION - A non-floating gate electrode (130) is set on a gate oxide (124) set on the bottom of the trench formed on a semiconductor substrate. An INDEPENDENT CLAIM is also included for an electronic system.

Basic Abstract Text (3):
USE - Used in manufacturing semiconductor wafers.

Basic Abstract Text (6):
Oxide spacers 122A,122B

Standard Title Terms (1):
INSULATE GATE FIELD EFFECT TRANSISTOR OXIDE SPACE SET NON FLOAT GATE ELECTRODE OPPOSED SIDEWALL TRENCH

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw. Desc | Image

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7. Document ID: JP 2002536833 W WO 200046858 A1 FR 2789519 A1 EP 1153435 A1

L1: Entry 7 of 15 File: DWPI Oct 29, 2002

DERWENT-ACC-NO: 2001-015477
DERWENT-WEEK: 200274

TITLE: Dynamic threshold MOS transistor device for low voltage applications, comprising current limiting device connected between transistor gate and channel

Basic Abstract Text (1):
NOVELTY - The semiconductor device integrated on a substrate comprises a first MOS transistor (10) with dynamic threshold voltage, having a gate (116) and a channel (111) of the first type conductivity, and a current limiting device (20) connected between the gate and the channel of the first transistor. The first MOS transistor is provided with a first region (160) doped with the first type conductivity connected to the channel, and the current limiting device comprises a second region (124) doped with the second type conductivity, disposed opposite to the first region, and electrically connected to the first region by an ohmic link in the form of a conductor layer. The current limiting device is a second MOS transistor (20), wherein the second region (124) and a third region (122) doped with the same type conductivity form the source and the drain of the second transistor.

Basic Abstract Text (2):
DETAILED DESCRIPTION - The second MOS transistor comprises a gate (126) connected to a contact (127) for the gate bias; the gate (126) is connected to the second doped region (124). The third doped region (122) is connected to the gate (116) of the first MOS transistor (10). The current limiting device can be in the form of a diode comprising second and third regions doped with opposite type conductivities. The device also comprises a fourth region (121), disposed between the second and the third regions and doped with the same type conductivity as one of the regions, but with a lower doping level. The invention comprises six embodiments, including the preferred embodiment; three embodiments are with the current limiting device in the form of transistor, and three other embodiments are with the current limiting device in the form of diode. The manufacturing method comprises the following steps: (a) the preparation of an active region (102) in substrate for receiving the first and the second transistors (10,20); (b) the formation of the first and the second gates (116,126) on the active zone, which are separated from the substrate by the gate insulator and cover the channel regions (111,121); (c) the formation of the first and the second regions of the source and the drain (112,114,122,124), by ionic implantation auto-aligned to the first and the second gates, and the formation of the first region (160), doped with the first type conductivity, in contact with the channel (111) of the first transistor, and adjacent to one of the regions of the source and the drain of the second transistor; (d) the formation of a conductor layer in electrical contact with the first doped region and one of the regions of the source and the drain of the second transistor. After completing step (d), an insulator layer of material as silicon oxide is deposited by planarisation on the substrate. The active zone is demarcated by the technology of localised oxidation of silicon (LOCOS) or shallow trench isolation, and doped with the first type conductivity. The formation of the conductor layer is preceded by the formation of lateral gate spacers, for the prevention of short-circuit between gates and the regions of source and the drain. The conductor layer is that of silicide, eg. $TiSi_2$ or $CoSi_2$, obtained by deposition of titanium or cobalt on silicon and thermal treatment.

Basic Abstract Text (3):
USE - In MOS transistors with insulated gate and with dynamic threshold voltage, namely in Dynamic Threshold Metal-Oxide-Semiconductor (DTMOS) transistors, for semiconductor implementation as silicon on insulator (SOI), comprising a thin upper layer of silicon insulated by an oxide layer; in CMOS circuits functioning with low supply voltages for use in microprocessors and digital signal processors (DSPs).

Basic Abstract Text (5):
DESCRIPTION OF DRAWING(S) - The drawing is a scheme for semiconductor implementation of the transistor circuit.

☐ 8. Document ID: US 6057194 A

L1: Entry 8 of 15 File: DWPI May 2, 2000

DERWENT-ACC-NO: 2000-338607
DERWENT-WEEK: 200104

TITLE: Formation of an insulated-gate field-effect transistor for integrated circuits includes forming a trench array, spacers in the second y-direction trench, gate insulator, gate electrode, source, and drain

Basic Abstract Text (1):
NOVELTY - An insulated-gate field-effect transistor is formed by forming a) a trench array; b) two spacers in the second y-direction trench; c) a gate insulator on the bottom surface of the second y-direction trench; d) a gate electrode on the gate insulator and the spacers; e) a source in the first and a drain in the second substrate region under the bottom surface.

Basic Abstract Text (2):
DETAILED DESCRIPTION - Forming an insulated-gate field-effect transistor (IGFET) in combination with a trench array comprises forming a) two x-direction trenches (120, 122, 124) and three y-direction trenches (130, 132, 134, 136, 138) that are orthogonal to and intersect with the x-direction trenches in a top surface (104) of a substrate (102), the x and the first two of the y-direction trenches surround a rectangular region (102A) of the substrate and the two x-direction trenches and the second and third y-direction trenches surround another rectangular region (102H) of the substrate, and the second y-direction trench is between the two substrate regions; b) two spacers in the second y-direction trench adjacent to the two substrate regions respectively; c) a gate insulator on a bottom surface of the second y-direction trench; d) a source on one substrate region and a drain (102B) in another both beneath the bottom surface. An INDEPENDENT CLAIM is also included for a method of forming an IGFET in combination with a trench array including applying an anisotropic etch to simultaneously form four isolation trenches and a transistor trench in a top surface of a semiconductor.

Basic Abstract Text (4):
ADVANTAGE - All the trenches are formed simultaneously using a single etch step.

Basic Abstract Text (5):
DESCRIPTION OF DRAWING(S) - The figures show the formation of insulated-gate field-effect transistor.

Basic Abstract Text (11):
X-direction trenches 120, 122, 124

Basic Abstract Text (12):
Y-direction trenches 130, 132, 134, 136, 138

Standard Title Terms (1):
FORMATION INSULATE GATE FIELD EFFECT TRANSISTOR INTEGRATE CIRCUIT FORMING TRENCH ARRAY SPACE SECOND DIRECTION TRENCH GATE INSULATE GATE ELECTRODE SOURCE DRAIN

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments   KWIC | Draw Desc | Image

☐ 9. Document ID: US 6005272 A

L1: Entry 9 of 15 File: DWPI Dec 21, 1999

DERWENT-ACC-NO: 2000-115423
DERWENT-WEEK: 200039

TITLE: Insulated-gate field effect transistors (IGFET) formation method for use in integrated circuit chips and electronic systems

Basic Abstract Text (1):
NOVELTY - An insulated-gate field effect transistor includes a source contact which is formed in the trench that is electrically coupled to the source at the bottom surface of the trench to improve packing density.

Basic Abstract Text (2):
DETAILED DESCRIPTION - An insulated-gate field effect transistor (IGFET) comprises a substrate including a trench with a bottom surface and two opposing sidewalls, a gate insulator on the bottom surface, a gate electrode on the gate insulator, insulative spacers between the gate electrode and the sidewalls, a source and a drain in the substrate and adjacent to the bottom surface and a source contact and a drain contact.

Basic Abstract Text (3):
An INDEPENDENT CLAIM is also included for an IGFET comprising a semiconductor substrate doped a first conductivity type, a gate insulator, a gate electrode which is spaced from and electrically isolated from the substrate and is closer to the second sidewall than to the first sidewall, a source doped a second conductivity type in the substrate, a drain doped the second conductivity type in the substrate, a channel doped the first conductivity type in the substrate, a source and drain contacts and three insulative spacers.

Basic Abstract Text (4):
USE - The invention is used for fabricating N-channel and P-channel metal oxide semiconductor field-effect transistors (MOSFETs), and other types of IGFETs, particularly for high-performance microprocessors where high circuit density is essential. The IGFET is used in an integrated circuit chip and in an electronic system, which also includes a microprocessor, a memory, a system bus (claimed).

Basic Abstract Text (5):
ADVANTAGE - The IGFET can have a channel length that is significantly smaller than the minimum resolution of the available lithographic system, thereby providing a next generation transistor with the present generation lithography. The gate electrode is aligned with the top surface of the substrate and the source contact overlaps the trench, improving packing density.

Standard Title Terms (1):
INSULATE GATE FIELD EFFECT TRANSISTOR IGFET FORMATION METHOD INTEGRATE CIRCUIT CHIP ELECTRONIC SYSTEM

☐ 10. Document ID: US 5915183 A

L1: Entry 10 of 15 File: DWPI Jun 22, 1999

DERWENT-ACC-NO: 1999-370613
DERWENT-WEEK: 199931

TITLE: Logic device with raised source-drain junctions

Basic Abstract Text (1):

NOVELTY - A semiconductor substrate contains at least 2 shallow trench isolation (STI) elements with a pad oxide layer covered by a nitride layer on the substrate between them. A portion of the nitride layer is etched to expose a portion of the pad oxide layer, and is replaced with a gate insulator. Polysilicon is deposited over the gate insulator in the gate conductor trench to form a gate conductor. The nitride layer is removed from between the gate conductor and the 2 STI elements to expose sidewalls of the gate conductor and the STI elements, on which insulation spacers are formed defining 2 source/drain trenches on opposite sides of the gate conductor. Intrinsic polysilicon is blanket deposited to fill the source/drain trenches and to cover the spacers and the 2 STI elements. The polysilicon is chemical mechanical polished to expose at least a portion of each of the spacers, and to planarize it in the source/drain and gate conductor trenches. The planarized polisilicon is recessed in the source/drain and gate conductor trenches, each recess being defined by 2 of the spacers and a recessed polysilicon surface. The recessed polysilicon is doped, and a salicide formed in the recesses on the doped polysilicon to form a salicide gate conductor and raised source/drain junctions.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments

KWIC | Draw Desc | Image

☐ 11. Document ID: KR 99030576 A KR 245271 B1 US 6162690 A

L1: Entry 11 of 15 File: DWPI May 6, 1999

DERWENT-ACC-NO: 2000-335897
DERWENT-WEEK: 200118

TITLE: Manufacture of field effect transistors, e.g. complimentary metal-oxide semiconductor, involves forming a conductive layer of first conductivity type on the face, sidewall and upper surface of insulated gate electrode

Basic Abstract Text (1):
NOVELTY - A field effect transistor is manufactured by forming a conductive layer of first conductivity type on the face and on a sidewall and upper surface of the insulated gate electrode. Dopants of first conductivity type are diffused from the conductive layer to the semiconductor region to define source and drain regions.

Basic Abstract Text (2):
DETAILED DESCRIPTION - Manufacture of a field effect transistor comprises: forming an insulated gate electrode (104) on a face of a substrate (100) containing a trench isolation region (102). A conductive layer (110a, 110b) of first conductivity type is formed on the face and on a sidewall and upper surface of the insulated gate electrode. Dopants of first conductivity type are diffused from the conductive layer to the semiconductor region to define source and drain regions. A first interlayer insulating layer (114) is formed on the conductive layer. An intermediate source (112a) and drain (112b) contact is formed by planarizing the first interlayer and the conductive layer, until the upper surface of the insulated gate electrode is exposed. The planarized conductive layer is etched back using the planarized first interlayer insulating layer as an etching mask. An electrode electrically coupled to the intermediate source/drain contact is formed.

Basic Abstract Text (3):
USE - The method is used for the formation of field effect transistor, e.g. complimentary metal-oxide semiconductor (CMOS), nMOS, and pMOS.

Basic Abstract Text (7):
Trench isolation region 102

Basic Abstract Text (8):
Insulated gate electrode 104

Basic Abstract Text (10):
Gate insulating spacers 108

Equivalent Abstract Text (1):
NOVELTY - A field effect transistor is manufactured by forming a conductive layer of first conductivity type on the face and on a sidewall and upper surface of the insulated gate electrode. Dopants of first conductivity type are diffused from the conductive layer to the semiconductor region to define source and drain regions.

Equivalent Abstract Text (2):
DETAILED DESCRIPTION - Manufacture of a field effect transistor comprises: forming an insulated gate electrode (104) on a face of a substrate (100) containing a trench isolation region (102). A conductive layer (110a, 110b) of first conductivity type is formed on the face and on a sidewall and upper surface of the insulated gate electrode. Dopants of first conductivity type are diffused from the conductive layer to the semiconductor region to define source and drain regions. A first interlayer insulating layer (114) is formed on the conductive layer. An intermediate source (112a) and drain (112b) contact is formed by planarizing the first interlayer and the conductive layer, until the upper surface of the insulated gate electrode is exposed. The planarized conductive layer is etched back using the planarized first interlayer insulating layer as an etching mask. An electrode electrically coupled to the intermediate source/drain contact is formed.

Equivalent Abstract Text (3):
USE - The method is used for the formation of field effect transistor, e.g. complimentary metal-oxide semiconductor (CMOS), nMOS, and pMOS.

Equivalent Abstract Text (7):
Trench isolation region 102

Equivalent Abstract Text (8):
Insulated gate electrode 104

Equivalent Abstract Text (10):
Gate insulating spacers 108

Standard Title Terms (1):
MANUFACTURE FIELD EFFECT TRANSISTOR METAL OXIDE SEMICONDUCTOR FORMING CONDUCTING LAYER FIRST CONDUCTING TYPE FACE SIDEWALL UPPER SURFACE INSULATE GATE ELECTRODE

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments   KWIC | Draw Desc | Image

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☐ 12. Document ID: US 5796143 A

L1: Entry 12 of 15 File: DWPI Aug 18, 1998

DERWENT-ACC-NO: 1998-466786
DERWENT-WEEK: 200029

TITLE: IGFET in combination with trench array - includes substrate with two x-direction trenches and three y-direction trenches defining two rectangular source/drain regions

Basic Abstract Text (1):
The IGFET includes a semiconductor substrate (102) with first and second x-direction trenches and first, second and third y-direction trenches (130,132,134,136,138). The x-direction trenches and the first and second y-direction trenches surround a first generally rectangular region of the substrate. The x-direction trenches and the second and third y-direction trenches surround a second generally rectangular region of the substrate. The second y-direction trench is between the two substrate regions.

Basic Abstract Text (2):
A gate insulator is on the bottom surface of the second y-direction trench. First and second spacers are in the second y-direction trench and adjacent to the first and second substrate regions, respectively. A gate electrode is on the gate insulator and the spacers. A source is in the first substrate region and beneath the bottom surface. A drain is in the second substrate region and beneath the bottom surface.

Basic Abstract Text (3):
ADVANTAGE - Allows an IGFET to have a channel length that is significantly smaller than the minimum resolution of the available lithographic system. Provides a gate electrode that is aligned with the top surface of the substrate. Produces trenches without additional processing steps. Allows selected gate electrodes and/or source/drain regions to be interconnected without the need for an overlying metallisation pattern.

Standard Title Terms (1):
IGFET COMBINATION TRENCH ARRAY SUBSTRATE TWO DIRECTION TRENCH THREE DIRECTION TRENCH DEFINE TWO RECTANGLE SOURCE DRAIN REGION

Additional Indexing Term (1):
INSULATED GATE BIPOLAR FIELD EFFECT TRANSISTOR

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments   KWIC | Draw Desc | Image

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☐ 13. Document ID: US 5250450 A

L1: Entry 13 of 15   File: DWPI   Oct 5, 1993

DERWENT-ACC-NO: 1993-328085
DERWENT-WEEK: 199341

TITLE: Insulated-gate vertical field-effect transistor mfr. - extending portion of conductive poly:silicon@ layer above surface of trench onto mesa to form gate contact

Basic Abstract Text (1):
The method involves forming a channel region and gate structure along the sidewall of trench in a P-type semiconductor substrate. The drain and source regions of the FET are formed in the mesa and the base portions of the trench. All contacts to the gate, drain, and source regions can be made from the top surface of the semiconductor substrate. One or more sidewalls of the trench are oxidised with a thin gate oxide dielectric layer followed by a thin polysilicon deposited film to form an insulated gate layer.

Basic Abstract Text (2):
A reactive ion etch step removes the insulated gate layer from the mesa and the base portions of the trench. An enhanced N-type implant creates the drain and source regions in the mesa and the base portions of the trench. The trench is partially filled with a spacer oxide layer to reduce gate-to-source overlap capacitance. A conformal conductive polysilicon layer is deposited over the insulated gate layer.

Standard Title Terms (1):
INSULATE GATE VERTICAL FIELD EFFECT TRANSISTOR MANUFACTURE EXTEND PORTION CONDUCTING POLY SILICON@ LAYER ABOVE SURFACE TRENCH MESA FORM GATE CONTACT

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments   KWIC | Draw Desc | Image

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☐ 14. Document ID: US 5122848 A

L1: Entry 14 of 15 File: DWPI Jun 16, 1992

DERWENT-ACC-NO: 1992-226232
DERWENT-WEEK: 199227

TITLE: Insulated-gate vertical field-effect transistor with high current drive - has drain and source regions formed in mesa and base portions of trench, with contacts on top surface and trench walls being oxidised

Basic Abstract Text (1):
The insulated-gate vertical FET has a channel region and gate structure that is formed along the sidewall of trench in a P-type semiconductor substrate. The drain and source regions of the FET are formed in the mesa and the base portions of the trench. All contacts to the gate, drain and source regions can be made from the top surface of the semiconductor substrate. One or more sidewalls of the trench are oxidised with a thin gate oxide dielectric layer followed by a thin polysilicon deposited film to form an insulated gate layer. A reactive ion etch step removes the insulated gate layer from the mesa and the base portion of the trench. An enhanced N-type implant creates the drain and source regions in the mesa and the base portions of the trench.

Basic Abstract Text (2):
The trench is partially filled with a spacer oxide layer to reduce gate-to-source overlap capacitance. A conformal conductive polysilicon layer is deposited over the insulated gate layer. A portion of the conductive polysilicon layer is extended above the surface of the trench onto the mesa to form a gate contact. A field oxide covers the entire surface of the FET, which is opened in the mesa to form gate and drain contacts and in the base to form the source contact.

Standard Title Terms (1):
INSULATE GATE VERTICAL FIELD EFFECT TRANSISTOR HIGH CURRENT DRIVE DRAIN SOURCE REGION FORMING MESA BASE PORTION TRENCH CONTACT TOP SURFACE TRENCH WALL OXIDATION

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments KWIC | Draw. Desc | Image

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☐ 15. Document ID: EP 282629 A DE 3782647 G EP 282629 B1 JP 63228742 A KR 9301221 B1 US 5025295 A

L1: Entry 15 of 15 File: DWPI Sep 21, 1988

DERWENT-ACC-NO: 1988-265150
DERWENT-WEEK: 198838

TITLE: Self-aligned contact of poly:silicon bit-line to diffusion - allows lower moat-depth for storage cells resulting in higher yield

Basic Abstract Text (1):
The storage cell arrangement consists of a moat-capacitor, pref. 4 micron deep and 0.8-1.0 micron wide, connected via a single transistor, formed on the surface, to the bit-line. The feature is that the bit-line contact (24) is self-aligned and partly overlaps on the field-oxide and the access gate-electrode (18). The gate-electrode is surrounded by insulator, with a spacer-oxide (20) pref. 200 nm wide at the bottom, and on top an oxide-layer (19). A triple layer of oxide, nitride and again oxide is deposited on the wafer to provide additional insulation (26) and an etch-stop (25), which is at least 10nm thick, and an underlying oxide-layer (29) pref. thicker than the nitride-layer.

Equivalent Abstract Text (1):
Three dimensional 1-transistor cell arrangement for dynamic semiconductor memories, in which the capacitor for the charges to be stored is constructed as a trench capacitor (9) in the substrate (1) and is arranged underneath the field-effect transistor (selection transistor), located on the surface of the common substrate (1), with an insulated gate electrode (transfer electrode/word line) and is electrically conductively connected to the source/drain zones (23) of said field-effect transistor, and in which the source/drain zones (23) of the field-effect transistor are made contact with on the exterior by a bit line (BL), this bit line (BL) being arranged above the plane containing the gate electrodes (18) and being isolated by means of an insulating layer (25,26,29), characterised in that (a) the bit line contact (24) for connection of the selection transistor is configured in a self-adjusting manner on the drain region (23) located in the semiconductor substrate (1), and in that the bit line contact overlaps the gate electrode (18), which is covered on all sides with insulating layers (19,20), and the adjacent field-oxide region (4), which is provided for lateral insulation of the individual elements of the circuit, (b) the insulation layer located under the bit line (BL) and above the gate plane consists of at least one double layer of silicon oxide (26) and silicon nitride (25), the layer adjacent to the bit line (BL) being a silicon oxide layer (26).

Equivalent Abstract Text (2):
A three dimensional one transistor semiconductor device has a doped substrate with a trench capacitor above which is a field effect transistor connected to the capacitor via the source or drain zone. The transistor having a switchable gate electrode on the surface. A bit line is spaced above the gate and insulated from it both by the insulating film and an intermediate insulating film of silicon oxide/silicon nitride/silicon oxide applied as a tripple layer. The silicon nitride layer is at least 10 microns thick but significantly thinner than the adjacent silicon oxide layers. Recesses allowing the bit line to be connected to the drain zone. ADVANTAGE - The device is compact while retaining reasonable levels of electrical efficiency. It can be produced in an uncomplicated way.

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Terms	Documents
semiconductor and (insulat$ adj gate) and trench and spacer	15

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Search Results - Record(s) 1 through 1 of 1 returned.

1. Document ID: JP 2002246596 A

L5: Entry 1 of 1 File: JPAB Aug 30, 2002

DOCUMENT-IDENTIFIER: JP 2002246596 A
TITLE: INSULATED GATE SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD

Abstract Text (1):
PROBLEM TO BE SOLVED: To reduce the unit cell area of a trench gate and to improve the withstand voltage of the gate.

Abstract Text (2):
SOLUTION: An insulated gate semiconductor device has a conductor layer for gate buried in a groove provided on a semiconductor substrate and another conductor layer for source on the main surface of the substrate. Part of a gate pillar composed of the conductor layer for gate and a cap insulating film covering the upper surface of the conductor layer is protruded onto the main surface of the substrate, and side wall spacers are provided on the side walls of the protruded potion of the gate pillar. The conductor layer for source is connected to the contact region of the main surface of the substrate specified by the side wall spacers. Since a source contact can be formed through self- alignment using the side wall spacers in this constitution, no margin is required for mask alignment and the area occupied by a unit cell can be reduced.

Applicant Name (2):
HITACHI TOBU SEMICONDUCTOR LTD

Applicant Name (Derived) (2):
HITACHI TOBU SEMICONDUCTOR LTD

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. Desc | Image

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Terms	Documents
semiconductor and (insulat$ adj gate) and trench and spacer	1

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Search Results - Record(s) 1 through 10 of 103 returned.

☐ 1. Document ID: US 6649954 B2

L7: Entry 1 of 103 File: USPT Nov 18, 2003

US-PAT-NO: 6649954
DOCUMENT-IDENTIFIER: US 6649954 B2

TITLE: Ferroelectric capacitor having upper electrode lamination

DATE-ISSUED: November 18, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Cross; Jeffrey S.	Kawasaki			JP

US-CL-CURRENT: 257/295

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

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☐ 2. Document ID: US 6642586 B2

L7: Entry 2 of 103 File: USPT Nov 4, 2003

US-PAT-NO: 6642586
DOCUMENT-IDENTIFIER: US 6642586 B2

TITLE: Semiconductor memory capable of being driven at low voltage and its manufacture method

DATE-ISSUED: November 4, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Takahashi; Koji	Kawasaki			JP

US-CL-CURRENT: 257/390; 257/308, 257/311, 257/315, 257/316, 257/322, 257/324, 257/331, 257/369, 257/391, 257/393, 438/128, 438/259, 438/270, 438/290

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

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☐ 3. Document ID: US 6638812 B2

L7: Entry 3 of 103 File: USPT Oct 28, 2003

US-PAT-NO: 6638812
DOCUMENT-IDENTIFIER: US 6638812 B2

TITLE: Method for producing a memory cell for a semiconductor memory

DATE-ISSUED: October 28, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Schlosser; Till	Dresden			DE
Hofmann; Franz	Munchen			DE

US-CL-CURRENT: 438/243

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

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☐ 4. Document ID: US 6628549 B2

L7: Entry 4 of 103 File: USPT Sep 30, 2003

US-PAT-NO: 6628549
DOCUMENT-IDENTIFIER: US 6628549 B2

TITLE: Semiconductor device

DATE-ISSUED: September 30, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Shukuri; Shoji	Koganei			JP
Yanagisawa; Kazumasa	Kokubunji			JP

US-CL-CURRENT: 365/185.24; 365/185.05, 365/185.14, 365/185.26

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw Desc | Image

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☐ 5. Document ID: US 6617623 B2

L7: Entry 5 of 103 File: USPT Sep 9, 2003

US-PAT-NO: 6617623
DOCUMENT-IDENTIFIER: US 6617623 B2

TITLE: Multi-layered gate for a CMOS imager

DATE-ISSUED: September 9, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Rhodes; Howard E.	Boise	ID		

US-CL-CURRENT: 257/215; 257/290, 257/291, 257/292, 257/59, 257/72, 257/E21.637

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw Desc | Image

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☐ 6. Document ID: US 6611636 B2

L7: Entry 6 of 103 File: USPT Aug 26, 2003

US-PAT-NO: 6611636
DOCUMENT-IDENTIFIER: US 6611636 B2

TITLE: Hybrid active electronic and optical Fabry Perot cavity

DATE-ISSUED: August 26, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Deliwala; Shrenik	Orefield	PA		

US-CL-CURRENT: 385/14; 398/141

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments   KWIC | Draw Desc | Image

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☐ 7. Document ID: US 6611019 B2

L7: Entry 7 of 103   File: USPT   Aug 26, 2003

US-PAT-NO: 6611019
DOCUMENT-IDENTIFIER: US 6611019 B2

TITLE: Method and structure for an improved floating gate memory cell

DATE-ISSUED: August 26, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Rudeck; Paul J.	Boise	ID		

US-CL-CURRENT: 257/315; 438/257

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments   KWIC | Draw Desc | Image

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☐ 8. Document ID: US 6608346 B2

L7: Entry 8 of 103   File: USPT   Aug 19, 2003

US-PAT-NO: 6608346
DOCUMENT-IDENTIFIER: US 6608346 B2

TITLE: Method and structure for an improved floating gate memory cell

DATE-ISSUED: August 19, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Rudeck; Paul J.	Boise	ID		

US-CL-CURRENT: 257/315

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments   KWIC | Draw Desc | Image

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☐ 9. Document ID: US 6599840 B2

L7: Entry 9 of 103 File: USPT Jul 29, 2003

US-PAT-NO: 6599840
DOCUMENT-IDENTIFIER: US 6599840 B2

TITLE: Material removal method for forming a structure

DATE-ISSUED: July 29, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Wu; Zhiqiang	Plano	TX		
Li; Li	Meridian	ID		
Figura; Thomas A.	Nishiwaki			JP
Parekh; Kunal R.	Boise	ID		
Pan; Pai-Hung	Boise	ID		
Reinberg; Alan R.	Westport	CT		
Ma; Kin F.	Boise	ID		

US-CL-CURRENT: 438/705; 257/E21.011, 257/E21.166, 257/E21.206, 257/E21.223, 257/E21.309, 257/E21.433, 257/E21.437, 257/E21.549, 257/E21.551, 257/E21.561, 257/E21.582, 257/E21.648, 257/E27.089, 438/752, 438/753

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments   KWIC | Draw Desc | Image

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☐ 10. Document ID: US 6596648 B2

L7: Entry 10 of 103 File: USPT Jul 22, 2003

US-PAT-NO: 6596648
DOCUMENT-IDENTIFIER: US 6596648 B2

TITLE: Material removal method for forming a structure

DATE-ISSUED: July 22, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Wu; Zhiqiang	Plano	TX		
Li; Li	Meridian	ID		
Figura; Thomas A.	Nishiwaki			JP
Parekh; Kunal R.	Boise	ID		
Pan; Pai-Hung	Boise	ID		
Reinberg; Alan R.	Westport	CT		
Ma; Kin F.	Boise	ID		

US-CL-CURRENT: 438/745; 257/E21.011, 257/E21.166, 257/E21.206, 257/E21.223, 257/E21.309, 257/E21.433, 257/E21.437, 257/E21.549, 257/E21.551, 257/E21.561, 257/E21.582, 257/E21.648, 257/E27.089, 438/692, 438/756

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments   KWIC | Draw Desc | Image

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